

# 2012 EOS/ESD Symposium for Factory Issues

## Compliance Verification of Static Dissipative Carrier for ESDS Devices in Semiconductor Backend Testing

**Micron Semiconductor Asia Pte Ltd**

Edmund SEAH, iNARTE Certified ESD Engineer (1st Author)

**Everfeed Technology Pte Ltd**

Yohan GOH, Application/Sales Manager (2nd Author)

Marcus KOH, ESDA Certified Professional, Program Manager (3rd Author)



# Objectives

- Use a verification method with simple & common practice for implementation in the factory
- Design a simple go/no-go compliance verification method for factory incoming material check
- Verify the consistency in the method
- Find a reliable method to verify the carrier's material ***static dissipative property*** consistently in an environment such as the production Line

# Outline

- In a typical ESD compliance verification, standard test method and tools are used in compliance to Standard (eg. ANSI/ESD S20.20)
- In manufacturing environment, such method may not provide consistent results quickly and reliably
- In this presentation, we are looking at a possible situation where a standard verification needs to be adapted

# MOTIVATION

- Electrostatic Sensitive (ESDS) semiconductor package transported around in an ***Electrostatic Safe Carrier***.

- The carrier holding the ESDS package transfers within **High-Temp** Test Handlers probes for testing.

- Charge Dissipated** by either via surface or volume carrier path.
- Static dissipative property**

- Carbon additive help create a dissipative path
- Carrier may not be homogeneous
- thus making material qualification challenging.

- Find a way to verify the carrier's material **static dissipative properties** with consistency in the production line to reduce the failure on the tester board due to ESD

# Equipment

- Surface Resistance Meter (SRM) - ANSI/ESD STM 11.11 & 11.12 compliance
- 2-pieces of 10-foot Silicone Test Lead (highly insulative type)
- Miniature 2 point probe - ANSI/ESD STM11.13 compliance
- Automated Handler Thermal Plastic Chip Carrier

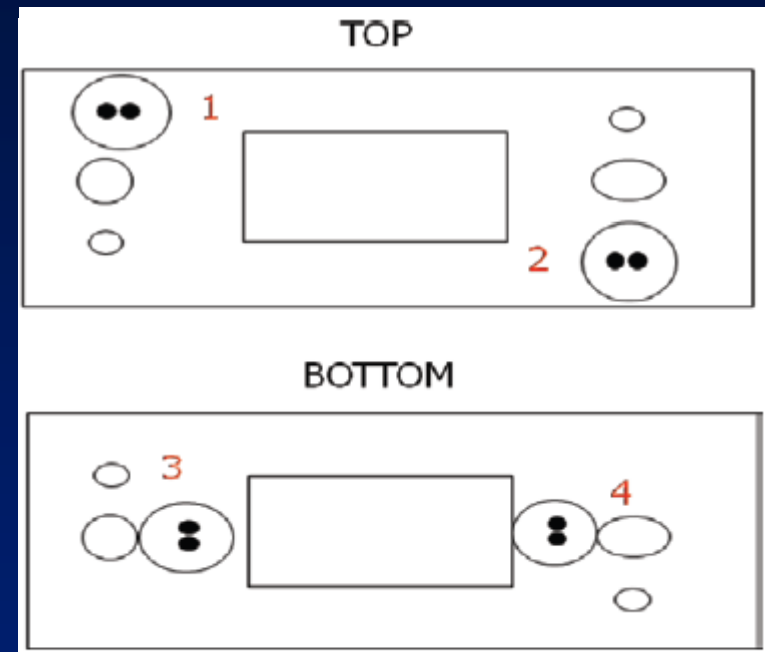
# METHOD 1



1. Plug 2 leads into the alternate corner hole of the chip carrier snugly
2. Turn on the SRM and perform measurement (10V & 100V)
3. Plug and unplug the leads and take down the measurement value for 5 times

# METHOD 2

- Use 2-points probe to measure 4 different position on the Chip Carrier
- Record the measurement with 3 attempts
- Perform average for each point



Probe Position on the device carrier

# Method 1 Measurement

The table shows the average measurement for each chip carrier using the test lead method

All the measurement falls within the expected E+04 to E+05 ohms

	item	ohm
Test Lead Method	1	1.24E+06
	2	9.41E+05
	3	7.68E+05
	4	1.06E+06
	5	6.48E+05
	6	7.92E+05
	7	7.73E+05
	8	6.69E+05
	9	6.66E+05
	10	8.16E+05



# Method 2 Measurement

	item	P1	P2	P3	P4
Hand held 2 point probe	1	6.17E+09	5.49E+09	1.03E+10	1.80E+06
	2	1.27E+10	3.90E+09	5.72E+08	8.84E+09
	3	1.13E+10	2.85E+05	1.80E+10	3.02E+09
	4	7.82E+05	2.57E+10	8.46E+09	2.05E+10
	5	3.15E+10	1.08E+10	4.82E+07	6.38E+07
	6	4.60E+09	1.70E+12	1.85E+10	1.00E+12
	7	2.00E+12	2.00E+12	2.00E+12	2.74E+08
	8	E12	E12	E12	E12
	9	E12	E12	E12	E12
	10	E12	E12	E12	E12

With Hand held 2-point probe, measurement are not consistency due to  
probe pressure, probe contact angle and chip carrier location

# Method 2 Measurement

A jig was made to address previous concerns and measurement are more consistent on the same test locationm, measurement are not reliable



	item	P1	P2	P3	P4
ESD jig	1	6.50E+05	7.10E+05	1.80E+11	3.20E+10
	2	8.20E+05	5.20E+09	3.10E+12	3.40E+12
	3	4.60E+05	5.90E+05	2.60E+12	4.10E+12
	4	4.80E+05	7.60E+05	1.50E+10	3.40E+12
	5	1.60E+05	1.60E+09	3.50E+12	3.70E+12
	6	2.20E+05	6.20E+05	3.90E+12	4.00E+12
	7	4.90E+05	4.50E+05	3.10E+12	3.40E+12
	8	9.30E+04	1.00E+09	3.50E+12	1.60E+11
	9	2.70E+05	4.30E+05	3.80E+12	3.10E+12
	10	1.80E+05	8.70E+05	3.00E+12	3.80E+12

# Results

- Base on the **method 1** measurement, carriers can be verified and sorted out in production floor as acceptable and non-acceptable (GO/NO GO).
- However, using **method 2** the data collected did not appear to be consistent
- For example, one sample 4 points measured, and a particular point could be ~E11 ohm while the rest are E6 ohm – non conclusive
- The method also depends on pressure, compression and etc. However, to reduce the physical differences, a jig was fabricated to perform the measurement

# Conclusion

- **Method 1** using the leads plug method is easy and provides a definitive Go/NO-GO decision matrix with very good repeatability
- **Method 2**, although is conforming to the recommended standard ANSI/ESD STM11.13, the measurement was not consistent and conclusive even with a placement jig

# Reference and Acknowledgement

- [1] ESDA, "ANSI/ESD S20.20-2007," in *Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)*, ed. June 24, 2007: ESD Association, 2007, p. 21.
- [2] ESDA, "ANSI/ESD S541-2003," in *Packaging Materials for ESD Sensitive Items*, ed. Mar 25, 2003: ESD Association, 2003, p. 21.
- [3] A. C. Pfahni, J. H. V. Lienhard, and A. H. Slocum, "Temperature control of a handler test interface," in *Test Conference, 1998. Proceedings., International*, 1998, pp. 114-118.
- [4] A. C. Pfahni, J. H. V. Lienhard, and A. H. Slocum, "Maximizing handler thermal throughput with a rib-roughened test tray," in *Test Conference, 1998. Proceedings., International*, 1998, pp. 109-113.
- [5] Z. Yuanheng, M. Hyman, C. Newberg, and K. Sagisaka, "Carbon nanotube plastic-packaging material for class 0 device ESD protection -Real life electrical performance comparison for carbon-filled plastics," in *Electrical Overstress/ Electrostatic Discharge Symposium, 2008. EOS/ESD 2008. 30th*, 2008, pp. 185-190.
- [6] ESDA, "ANSI/ESD STM11.11-2006 Surface Resistance Measurement of Static Dissipative Planar Materials," ed. Rome, NY, USA: ESD Association, 2006, p. 13.
- [7] ESDA, "ANSI/ESD STM11.12-2000 Volume Resistance Measurement of Static Dissipative Planar Materials," ed. Rome, NY, USA: ESD Association, 2000, p. 13.
- [8] ESDA, "ANSI/ESD STM11.13-2004 Two-Point Resistance Measurement," ed. Rome, NY, USA: ESD Association, 2004, p. 10.
- [9] XIAO Qiyue & Dexter GAY, Acknowledgement for Presentation Slides Preparation