Probabilistic Analytical Benchmarking for ESDS Manufacturing Process

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50 Words Abstract - A chronological ESD process analysis is proposed to identify the root cause of ESD sensitive devices' premature failure due to several field returns which exceeded customers' factory targeted ESD failure control threshold. Two novel quantitative ESD risk indices are proposed to benchmark the process ESD capability using probabilistic statistical technique.

I. Introduction

Given the advantage of lower cost per device driven by high volume production by semiconductor manufacturers, ESD Sensitive devices' (ESDSs) market price continues downwards with end-users increasing demand for lower cost,. All owners, semi-conductor or contract manufacturers have their own novel manufacturing work flow: through operators on bench top and automated handling equipment (AHE) to achieve tremendous cost benefits, productivity increase and fast turn-around time. Without compromising on ESDS catastrophic failure or latency issues, industrial key challenges are on changes or retention of operators as well as AHEs' availability and reliability. There is a lack in ESD capability benchmarking tool with quantitative evidences describing the past manufacturing ESD capability; much less predicting factory future ESD performance.

Section I narrates the need to lower ESD manufactured risks quantitatively using ESD risk indices via probabilistic method [1, 2]. Section II provides description on ESD process analysis of each process step: identify equipment with high ESD risk and attempt to mitigate. In section III, the two new ESD risk indices using probabilistic analytical technique (PAT) is presented. Section IV concludes this paper with findings.

II. ESD Process Analysis

A chronological-based ESD process analysis identifies the root cause in a back-end semiconductor manufacturing ESDS failures from customers exceeding targeted control threshold.

Figure 1 describes a typical process flow of a back-end semiconductor manufacturing

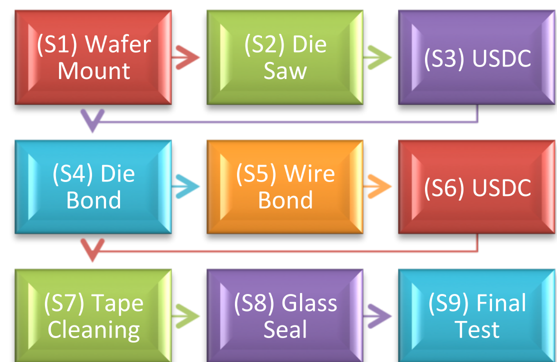

Figure 1 A typical process flow sequence in a back-end semiconductor manufacturing

The back-end semiconductor manufacturing process flow sequence for this investigation is from Step-1 (S1) to Step-9 (S9). The wafers mounted at S1 are then processed at die saw (S2). After die saw, the sawed wafer undergoes ultrasonic drying cleaner (USDC) at S3. The dried dies are mounted on lead frames at die bond (S4). Wire bond (S5) connect the wires from die pads to their corresponding location on lead frame. The ESDS will pass through another

USDC at S6 before tape cleaning at S7, glass sealing at S8 and eventual final testing at S9.

This new ESDS was first introduced locally in 3rd quarter 2013 with ≤ 0.05% control threshold of ESDS failures set per month. The time line chart in Figure 2 narrate the chronological sequences of four different customers' return starting from 21-Nov-2013, 17-Dec-2013, 21-Jan-2014 and 31-Jan-2014 abbreviated as P1, P2, P3 and P4 respectively. For P1, customer A1 return 54 failed ESDS found in their production line out of 30,000 giving 0.18% failure. Customer A2 and A3 each returned 1 failed ESDS captured in their production line as P2 and P3 respectively. Final customer A4 returned 14 failed ESDS, reported in their production line, as P4. These progressively returned ESDS were consistent with failure type C13 after failure analysis, where the normal C13 failure threshold pre-set in Figure 1 was 0.05% per month. After process mapping on the manufacturing line and detail failure analysis of ESDS, the dies map turned out to be crowded around a physical location on wafer, as indicated in red & yellow via Figure 3, and usually wafer #25.

The first conjecture for lower yield and high C13 failure was dust related issues, which led to dust containment strategy. All twenty-five wafers in cassette waiting in transits were placed vertically under cleanroom Class 10 environment with laminar flow ionization to avoid particles from settling on wafers' surface due to electrostatic attraction. Prior to die bonding process (S4), the wafers were enclosed in nitrogen storage box. However, these containment techniques did not resolve the high C13 failure issue over time.

A detail ANSI/ESD S20.20 [3] assessment was carried out along the process flow as Figure 1, to identify electrostatic discharge protected area (EPA) with high charge within vicinity of ESDS. The company ANSI/ESD S20.20 ESD Control Plan stipulates any electrostatic field greater than 100V within vicinity of ESDS shall be controlled. This was primarily investigated with electrostatic field meter and non-contact voltmeter.

At the integrated die saw (S2) equipment, there was a UV curing process step where wafer charge was >20kV. As there was no opportunity for ESDS to contact any metal surface after UV curing process step and subsequent process step can neutralize the high charge on wafer surface, this was categorized as a low ESD risk process step.

As such, much effort was spent on Die Bond (S4) in lowering the pick and place actions to lesser than 100V. However, the C13 failure exceeding threshold issue persisted over time.

Despite details ESD assessment & containment strategies on the root cause(s) of C13 failure, it was to no avail. Hence, the investigation returned to high charge areas in process step from S1 to S9. Since S2 was reported with high charge after UV curing, two counter actions were implemented. A clean dried compressed air (CDA) ionization bar [4-7] was placed between spin wash and UV curing process step within S2 in November 2013. Furthermore, wafer blowing time at S2 spin wash process step was increased from 1s to 3s allowing more exposure time to CDA air ionization. The surface charge on wafers reduced

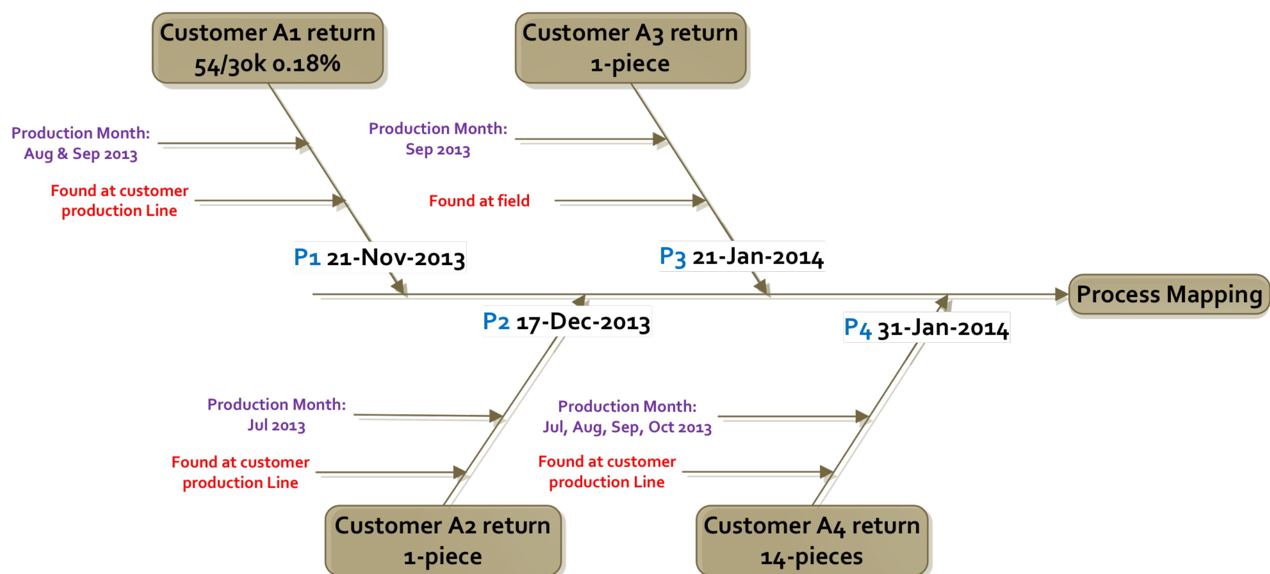

Figure 2 Chronological sequences of ESDS field returns from four customers

below 20V. Antistat was applied to a highly charged proximity sensor mounted very close to wafer #25 UV curve transit area to below 100V as in Figure 4. These counter measures have reduced C13 failure threshold to around the targeted control level.

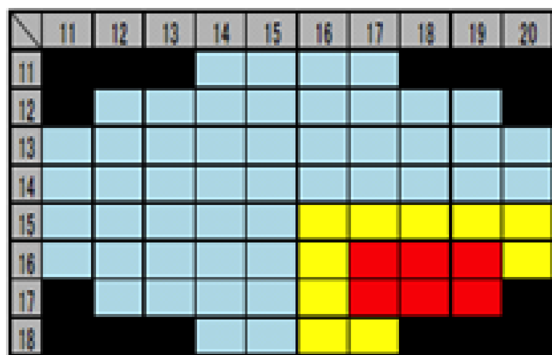

Figure 3 Reject wafer location

Figure 4 Sensor at S2 identified with charge >20kV

III. ESD Risk Indices

As all process steps are highly automated with information communication technology (ICT), adequate time series data has been collected on status of equipment operation status, and machine availability / unavailability [8-10]. These leads to the proposal of two novel quantitative ESD risk indices to benchmark the process ESD capability using probabilistic analytical technique (PAT) with time series data collected from the process.

Even with ANSI/ESD S20.20 program in place, devices' catastrophic ESD failure and latency problems could still persist. ESD is stochastic in nature which cannot be analysed deterministically. A better approach in analysing past behaviour and predicting future performance is probabilistic method for process ESD capability assessment or benchmarking. Using PAT with comprehensive ICT data analytics from equipment, two quantitative ESD risk indices can be formulated as benchmarking of factory ESD process capability. These indices can be used to compare between factories, between ESD Protected Areas (EPAs), between AHEs and/or between benchtops. Figure 5 shows the factory daily demand for this particular ESDS over an annual period. This can be sorted in descending as show in Figure 6, which is called the demand duration curve (DDC). If the factory ESDS supply capacity (red line) intercepts with DDC, the number of ESDS not produced to meet demand (θ_i) and the individual probability of this state (p_i) can be derived.

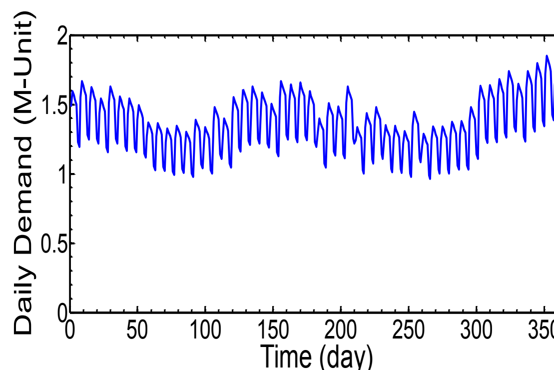

Figure 5 Factory annual ESDS Device demand time series

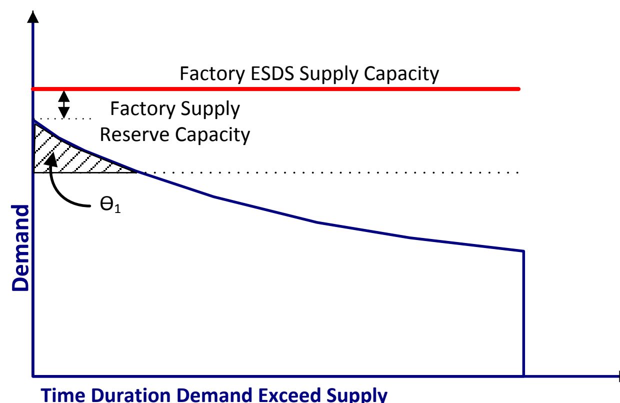

Figure 6 ESDS Devices unable to meet demand due to supply inadequacy

Loss of unit (ESDS Device) expectation (LOUE) is expressed in Million-Unit/year or (M-Unit/year). Equation (1) LOUE is the probability of units (ESDS Devices) not supplied is the area under DDC. The sum of these products is the total expected units not supplied, or loss of unit expectation. LOUE indicates the intensity of occurrence.

$$LOUE = \min \ \left\{\sum_{i=0}^{N} \theta_i * p_i\right\} \mathrm{M-Units/year} \qquad (1)$$

where,

p_i individual probability of process line ESDS supply capacity at i^{th} interval

S_i process line supply capacity at i^{th} interval (in M-Unit)

D_i process line demand at i^{th} interval (in M-Unit)

t_i occurrence (in time units for the period under study) where (process line supply is less than demand) at i^{th} interval

Loss of unit (ESDS Devices) expectation per unit (LOUEPU) is shown in (2). LOUEPU is normalized by utilizing the total units under the demand duration curve (DDC), i.e. $\theta = \sum_{i}^{N} \theta_{\boldsymbol{i}}$, as shown in Figure 6 where N is the total study period. The per unit LOUE value represents the ratio between the probability demand units not supplied due to deficiencies in the available factory supply capacity and to total demand units required to serve the customers' demand.

$$LOUEPU = \min \ \left\{\sum_{i=0}^{N} (\theta_i * p_i)/\theta\right\} \quad \mathrm{P.U.} \qquad (2)$$

IV. Conclusion

A chronological ESD process analysis has been implemented in tandem with best practices as per ANSI/ESD S20.20 to identify the root cause of high customer returns. Several process mapping has been carried out and the high probability of C13 ESDS failure on wafer #25 was identified. This has led to S2 equipment which has a proximity sensor measured greater than 20kV. An antistat coating is coated on the proximity sensor and the yield lost immediately dropped below control threshold. As all process steps are highly automated with information communication technology (ICT), adequate time series data has been collected on status of equipment operation status, and machine availability / unavailability. These leads to the proposal of two novel quantitative ESD risk indices to benchmark the process ESD capability using probabilistic analytical technique (PAT) with time series data collected from the process. LOUE and LOUEPU can be used for quantitative analysis for comparison between factories, between EPAs etc.

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