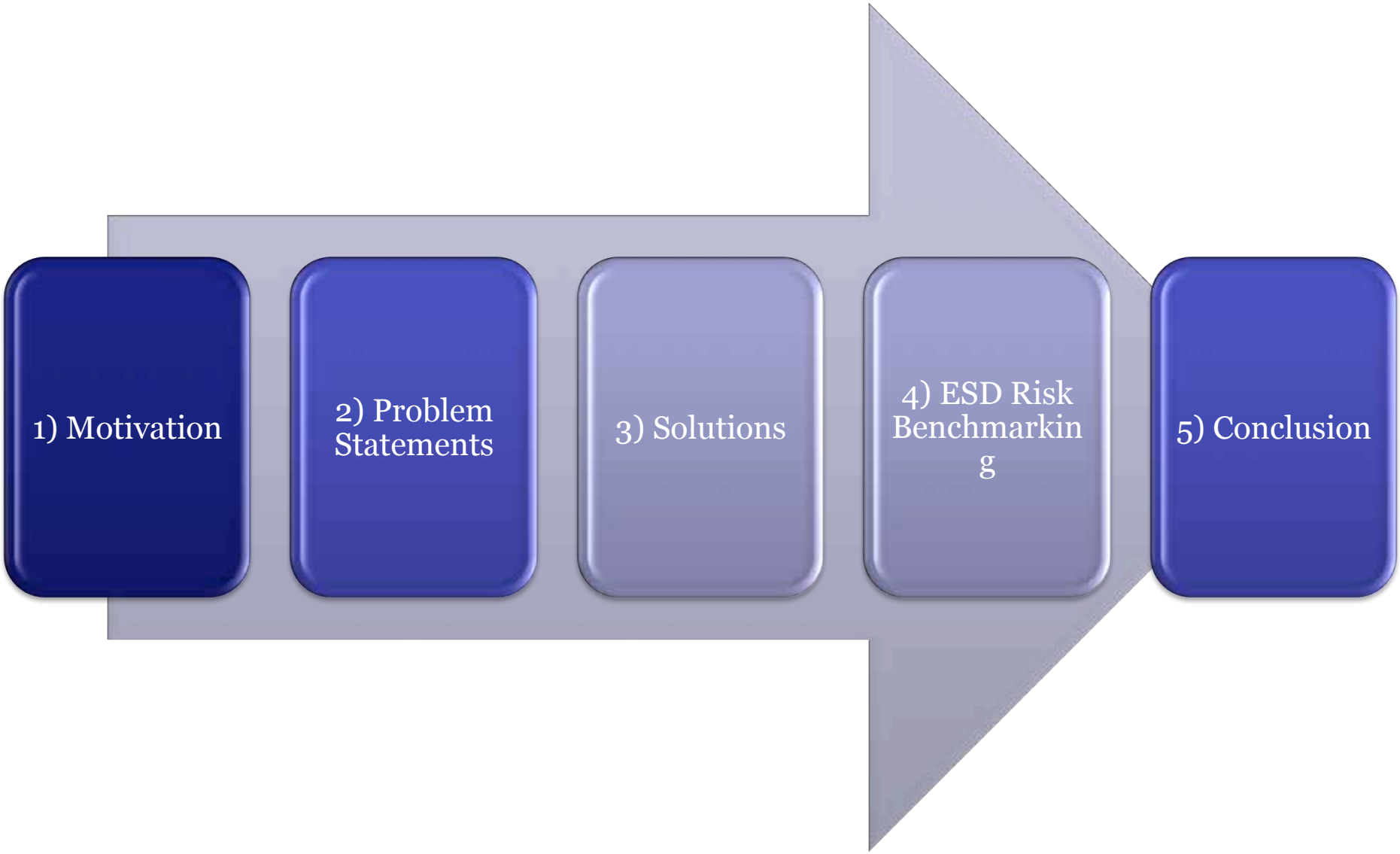
2014 EOS/ESD Factory Symposium

ESD Process Capability Analysis & Probabilistic Analytical Benchmarking

Marcus KOH (ESDA Certified Professional-Program Manager, Exemplar Global iNARTE Certified ESD Engineer),
Email: marcus_koh@everfeed.com.sg
Maurice GOH, Email: mgohcb@gmail.com
Yohan GOH, Email: Yohan_goh@everfeed.com.sg

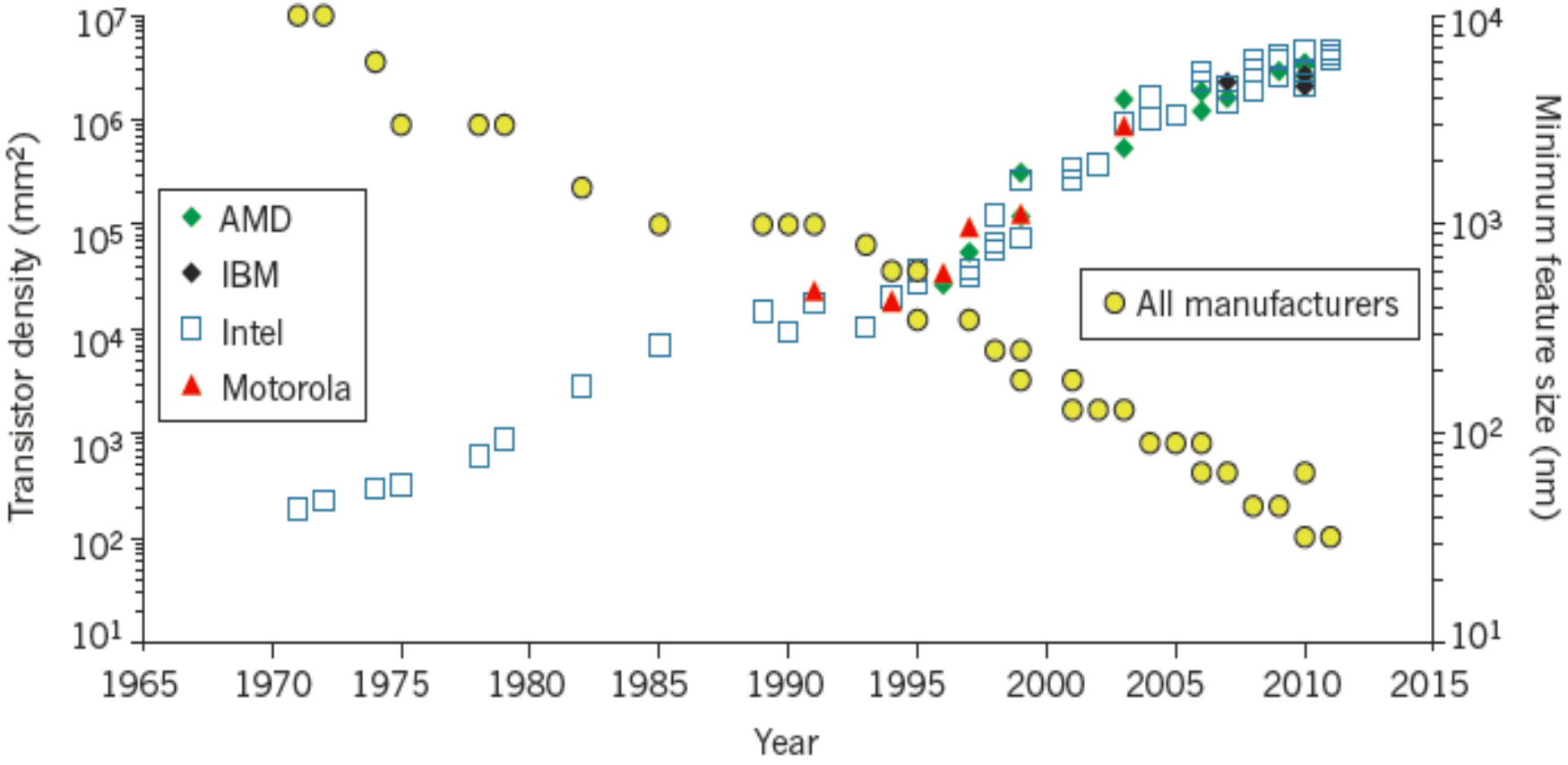
Overview


1) Motivation
2) Problem Statements
3) Solutions
4) ESD Risk Benchmarking
5) Conclusion

1.1) Motivation

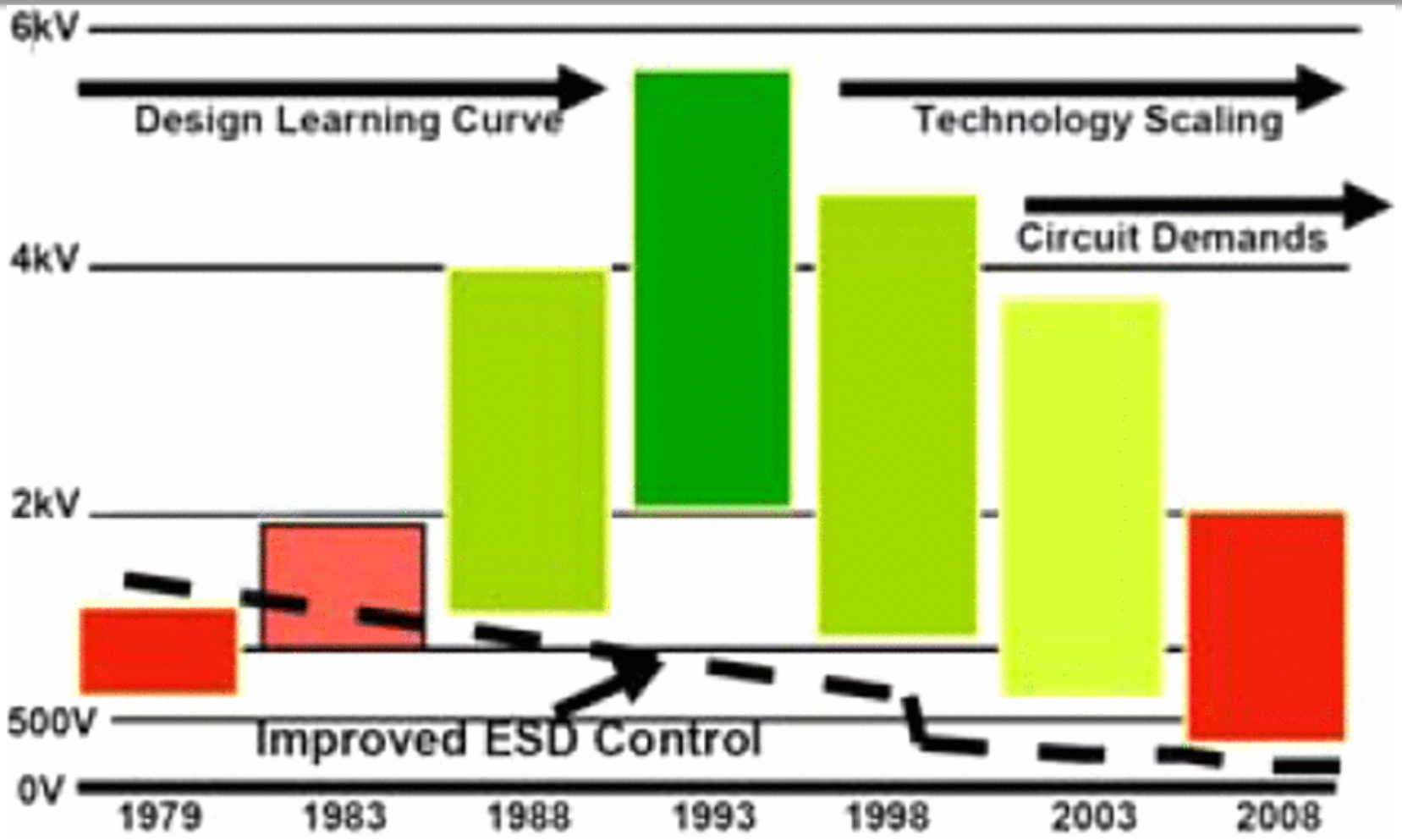
1. Rapid technology scaling placed too high a burden on ESD design. Traditional ESD protection circuits having problems.
2. Trade-offs between ESD design and protection levels no longer actively pursued -> HBM & CDM expected to be lowered -> catastrophic or latency issues.
3. Factory uncertainty of producing ESDS with catastrophic failure, or latency issues. How can one **quantitatively** determine ESD process capability in a factory for **hundreds of process** steps.

1.2) Motivation



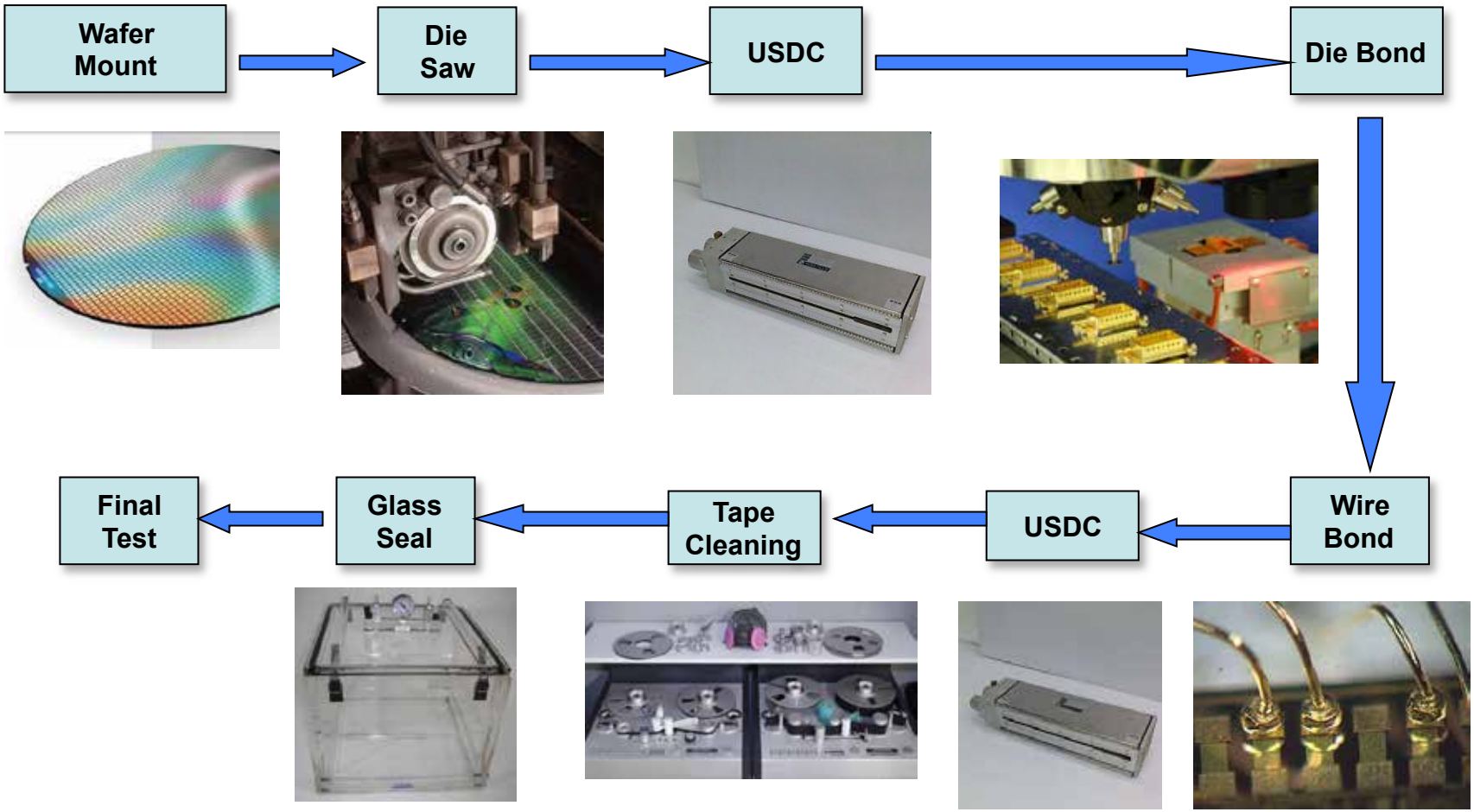
[7] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature,* vol. 479, pp. 310-316, 2011

1.3) Motivation

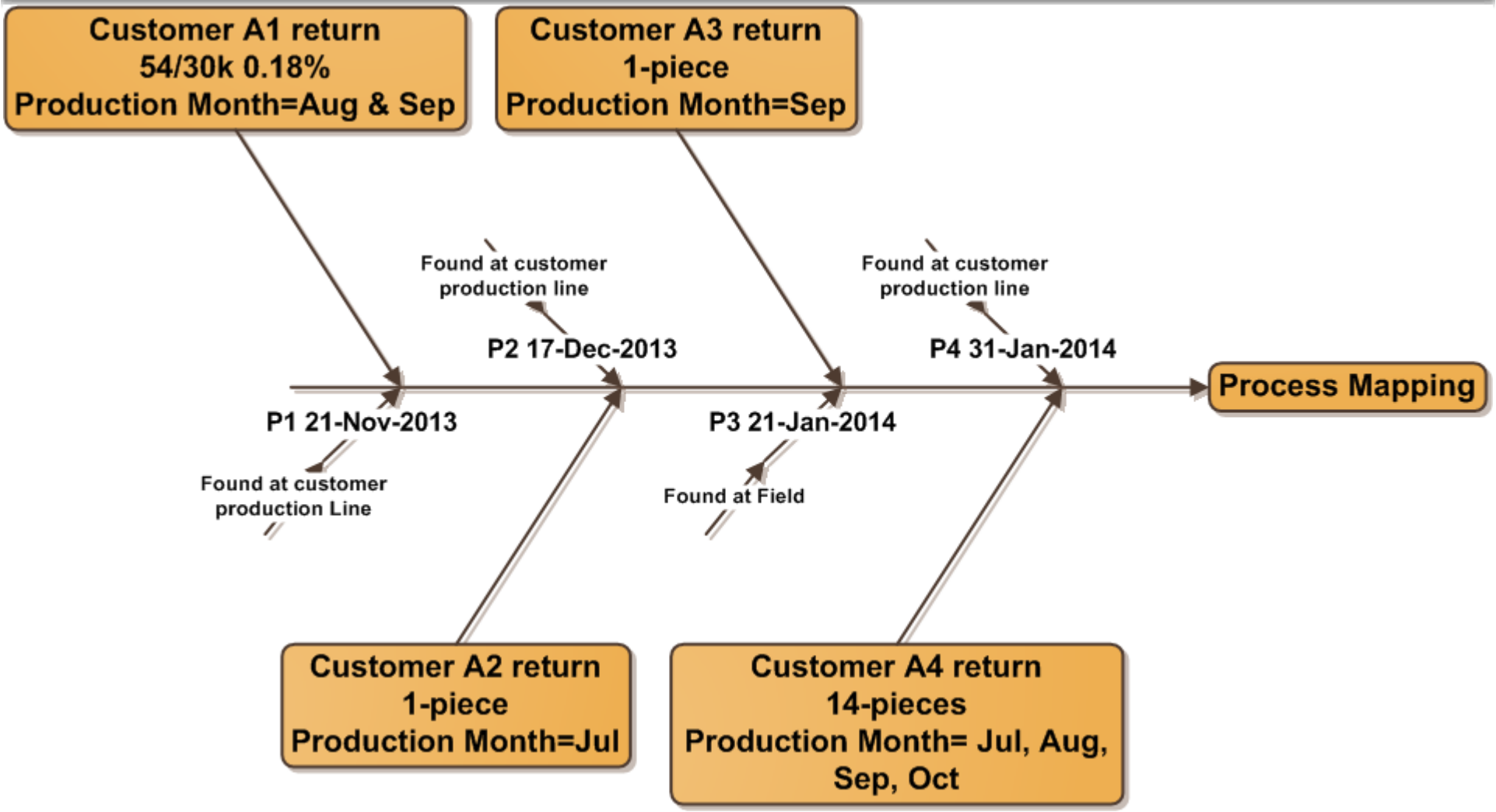


[6] S. Millar and J. Smallwood, "CDM damage due to Automated Handling Equipment," in *Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD), 2010 32nd*, 2010, pp. 1-8.

2.1) Problem Statement: Back end Semiconductor Manufacturing Process

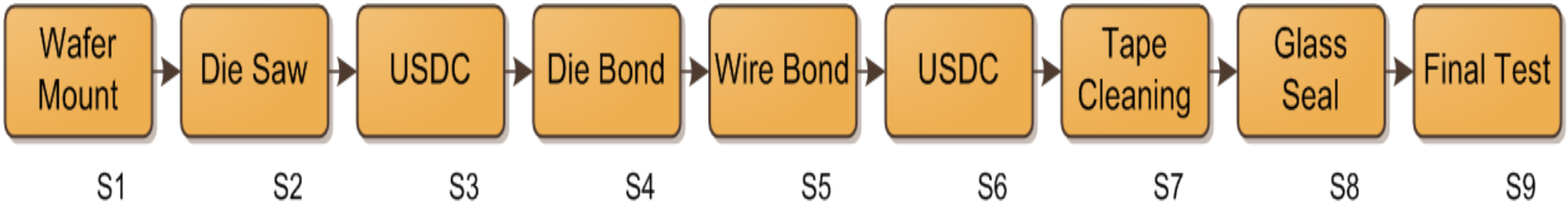


2.2) Problem Statement - Timeline



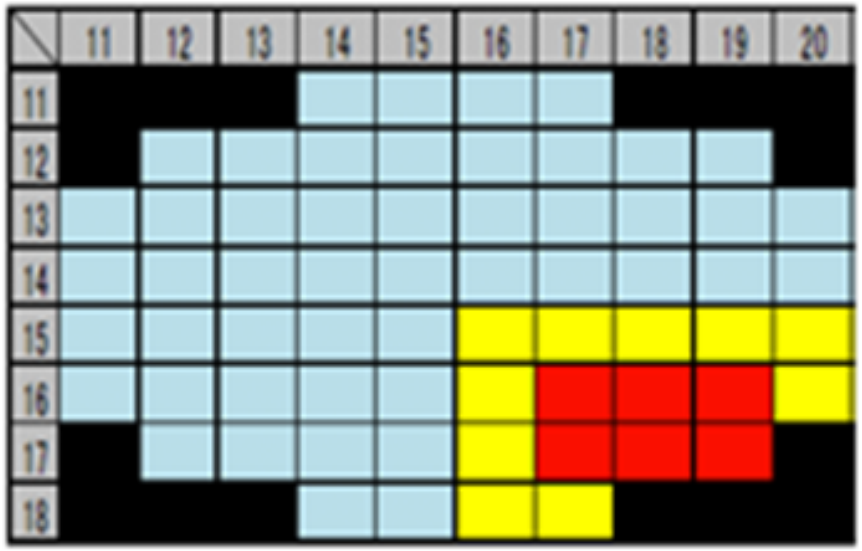
2.3) Problem Statement - Description

1. New ESDS device introduced in 3rd quarter 2013
2. Control threshold set at 0.05% or lower per month
3. From 12 Dec ~ 31 Jan, 4 isolated cases of returns due to ESDS failure.
4. 0.05% threshold exceeded by 1 customer



2.4) Problem Statement: Mapping

1. Process mapping + Detailed failure analysis --->> Failure type C13, only on Wafer# 25 in carrier



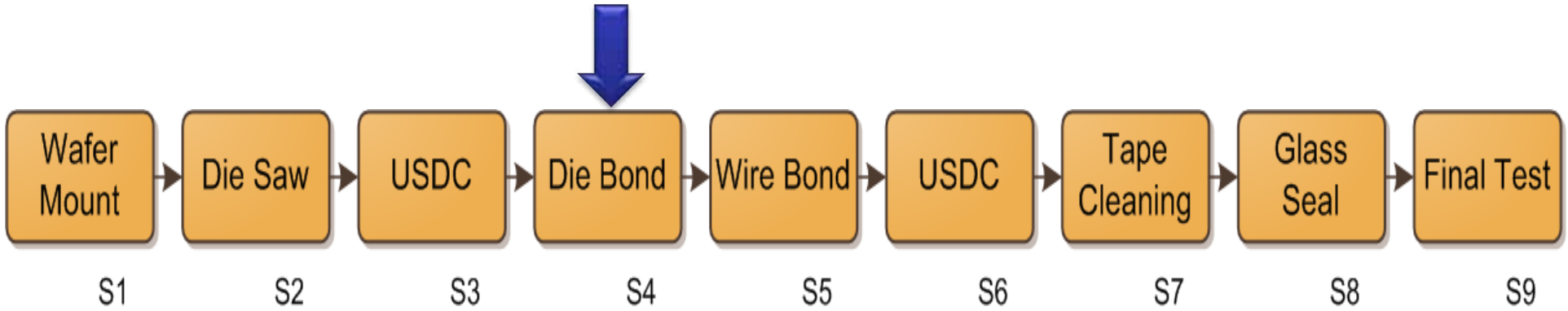
C13 Reject wafer location

2.5) Problem Statement: Conjecture

1. Preliminary Conjecture for lower yield/ high C13 failure : Dust related issues???
2. Proceed to devise dust containment strategies

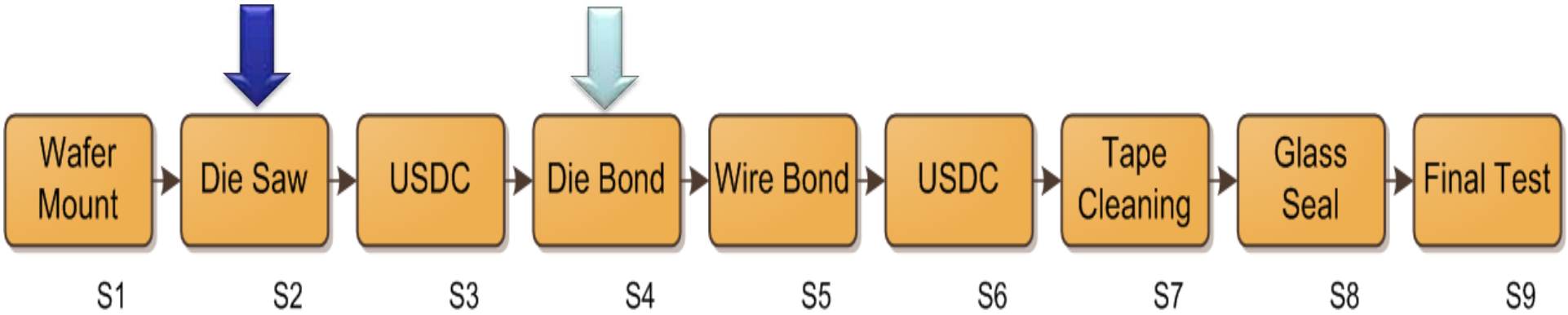
3.1) Solution I

1. Wafers in cassette waiting in transits placed vertically under clean room Class 10 environment to avoid settling of dust particles.
2. Prior to die bonding process (S4), wafers enclosed in nitrogen storage box.
3. Results ---> C13 failure persists



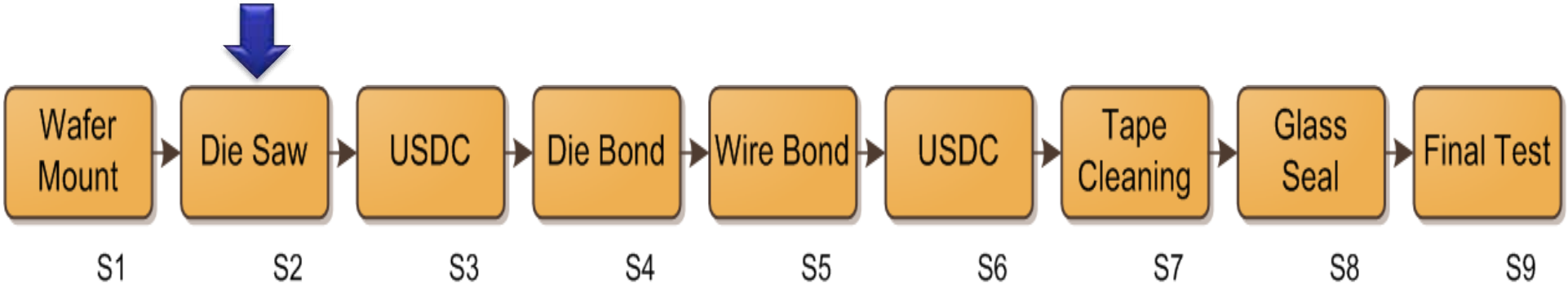
3.2) Solution II

1. Detail ANSI/ESD S20.20 carried out to identify EPA with high charge within vicinity of ESDS
2. UV curing process near S2, however, it is determined that ESDS has no risk of contact with any metal surface > low risk ESD risk process
3. Continued to lower charge at S4 <100V.
4. Results ---> C13 Failure persists.



3.3) Solution III

1. 2 countermeasures of high charge at S2
2. Increase in wafer blowing time from 1s to 3s for better ionisation exposure from clean dried compressed air (CDA)
3. Antistat applied to highly charged proximity sensor mounted close to wafer#25 UV transit area to below <100V
4. Results --->> C13 failure threshold reduced to ~0.05%



4.1) Process ESD Benchmarking

1. Most manufacturing factories have hundreds of automated handling machines & manual bench tops.
2. Process steps are highly automated with information communication technology (ICT), adequate data can be collected
3. Leads to the proposal of 2 novel quantitative ESD risk indices to benchmark the process ESD capability

4.2) Stochastic Problems

1. ESD is stochastic in nature and cannot be analysed deterministically.
2. Even with ANSI/ESD S20.20, catastrophic and latency ESD failures can still persist.
3. A better approach in analysing past data to predict future performance is the probabilistic method.
4. Propose 2 novel quantitative ESD risk indices to benchmark the process ESD capability for small to large factory size with hundreds of process steps.

4.3) Quantitative ESD Indices

1. Probabilistic Analytical Technique (PAT) + ICT -->> 2 quantitative ESD risk indices
   I. Loss of Demand Expectation (LODE) expressed in days/year
   II. Loss of Demand Probability (LODP) expressed in per unit (P.U.)

4.4) LODE & LODP

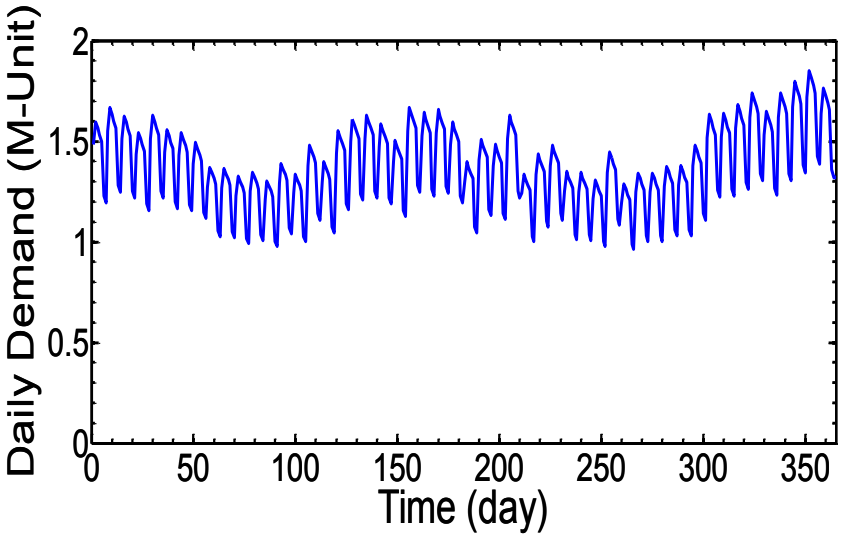
$$LODE = \min\left\{\sum_{i=0}^{n} t_i * p_i(S_i - D_i)\right\} \text{ days/year}$$

$$LODP = \min\left\{\sum_{i=0}^{n} p_i * (S_i - D_i)\right\} \text{ P.U./year}$$

p_i individual probability of process line supply capacity at i^{th} interval
S_i process line supply capacity at i^{th} interval
D_i process line demand at i^{th} interval
t_i occurrence where (process line supply < demand) at i^{th} interval due to ESD failures

1. LODE is an expectation of ESDS demand loss in time units for the period under study
2. LODP is expectation of ESDS demand loss probability in P.U. for the period under study.

4.5) ESD risk benchmarking



$$LODE = \min\left\{\sum_{i=0}^{n} t_i * p_i(S_i - D_i)\right\} \text{days/year}$$

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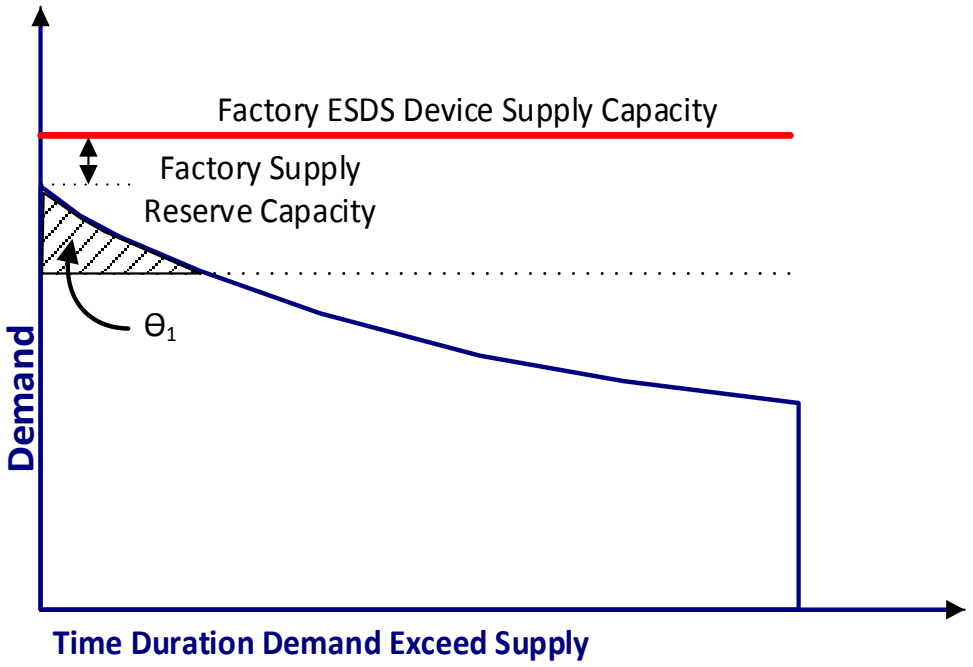

5) Conclusion

1. ESDS failure identified through process mapping and identified root cause -> S2 with high E-Field
2. Conventional process capability relies heavily on historical data & deterministic method on process ESD capability in question.
3. Modern factory with ICT data enables development of novel & quantitative ESD indices (LODE and LODP) using probabilistic analytical technique (PAT).
4. Different semiconductor manufacturers with hundreds of process steps can compare their internal factory (or factory-factory) ESD process capability quantitatively using PAT.

Acknowledgements

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Acknowledgements

Slide No 6 :

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